What is claim d is:

1. A precharge method in a semiconductor memory device having a hierarchical structure in which bitline pairs are connected with local input/output line pairs, and the local input/output line pairs are connected to global input/output line pairs, the method comprising:

precharging the global input/output line pairs with the half of a memory cell array voltage; and

precharging the local input/output line pairs with the half of the memory cell array voltage.

2. A semiconductor memory device having a hierarchical structure, comprising:

one pair of bitlines connected to a memory cell;

one pair of local input/output lines;

a column selector connected between the one pair of bitlines and the one pair of local input/output lines, for selecting a corresponding bitline in response to a column selection signal;

a local input/output line sense amplifier connected between the one pair of local input/output lines, for sensing and amplifying data of the one pair of local input/output lines in response to a local input/output line sense amplifier drive signal;

one pair of global input/output lines crosswise connected to the one pair of local input/output lines;

and

a write driver for receiving the data and loading the data on the one pair of global input/output lines, and a global input/output line precharge part for precharging the one pair of global input/output lines with a half of a memory cell array voltage in response to a global input/output line precharge signal,

wherein the one pair of local input/output lines is precharged with and dependently on the precharge by which the global input/output lines was precharged.

3. The device of claim 2, further comprising:

a bank selector connected between the one pair of global input/output lines, for selecting a corresponding bank in response to a bank selection signal;

a global input/output sense amplifier connected between the one pair of global input/output lines, for sensing and amplifying the data of the one pair of global input/output lines; and

a sense amplifier global input/output line precharge part connected between the bank selector and the global input/output sense amplifier, for precharging one pair of sense amplifier global input/output lines with half voltage the memory cell array voltage in response to a sense amplifier global input/output line precharge signal.

4. The device of claim 2, wherein each of the

precharge parts includes:

an NMOS transistor connected between the one pair of global input/output lines and driven by the global input/output line precharge signal; and

two NMOS transistors connected in series between the one pair of global input/output lines and driven by the global input/output line precharge signal, for providing the one pair of global input/output lines with the half voltage of the memory cell array voltage.

5. A semiconductor memory device having a hierarchical structure, comprising:

one pair of bitlines connected to a memory cell;

one pair of local input/output lines connected to the one pair of bitlines;

one pair of global input/output lines crosswise connected to the one pair of local input/output lines; and

a global input/output line precharge part for precharging the one pair of global input/output lines with a half voltage of a memory cell array voltage in response to a global input/output line precharge signal,

wherein the one pair of local input/output lines is precharged with and dependently on a voltage by which the global input/output lines were precharged.

6. The device of claim 5, wherein the precharge part

precharges the one pair of local input/output lines with the half voltage of the memory cell array voltage when precharging one pair of global input/output lines.

7. The device of claim 6, wherein the precharge part includes:

an NMOS transistor connected between the one pair of global input/output lines and driven by the global input/output line precharge signal; and

two NMOS transistors connected in series between the one pair of global input/output lines and driven by the global input/output line precharge signal, for providing the one pair of global input/output lines with the half voltage of the memory cell array voltage.